CLAIMS

What is claimed is:

1. A method comprising:

applying a first predetermined signal to a first wire;

applying a second predetermined signal to a second wire, wherein the second wire is parallel to the first wire; and

determining, based at least in part on a current signal, a cross coupling capacitance between the first wire and the second wire.

2. The method of claim 1 wherein the second predetermined signal comprises a constant voltage for a first period of time and a periodic signal for a second period of time.

3. The method of claim 1 wherein applying a first predetermined signal to the first wire further comprises:

applying a first periodic voltage to a first transistor; and

applying a second periodic voltage to the first wire via an inverter.

4. The method of claim 3 wherein the current signal corresponds to current flowing through the first transistor.

5. A machine readable storage medium having stored therein a plurality of machine executable instructions that implement a parasitic extraction tool that operates to generate electrical modeling data for an integrated circuit (IC) design, wherein the parasitic extraction tool includes a database of capacitance values, wherein the capacitance values are determined by:

evaluating a first predetermined signal on a first wire;

evaluating a second predetermined signal on a second wire; and

determining, based at least in part on a current signal, a cross coupling capacitance between the first wire and the second wire.

6. The machine readable medium of claim 5 wherein the second predetermined signal comprises a constant voltage for a first period of time and a periodic signal for a second period of time.

7. The machine readable medium of claim 5 further comprising determining, based at least in part on the current signal, a total capacitance of the first wire.

8. The machine readable medium of claim 5 wherein a first predetermined signal on the first wire comprises:

evaluating a first periodic current voltage to the first wire via a transistor; and

evaluating a second periodic current voltage to the first wire via an inverter.

9. The machine readable medium of claim 8 wherein the current signal corresponds to current flowing through the transistor.

10. A machine readable storage medium having stored therein a plurality of machine executable instructions that implement an integrated circuit (IC) design simulation tool, wherein the IC design tool simulates an IC design based on capacitance values determined by:

evaluating a first predetermined signal on a first wire;

evaluating a second predetermined signal on a second wire; and

determining, based at least in part on a current signal, a cross coupling capacitance between the first wire and the second wire.

11. The machine readable medium of claim 10 wherein the second predetermined signal comprises a constant voltage for a first period of time and a periodic signal for a second period of time.

12. The machine readable medium of claim 10 further comprising determining, based at least in part on the current signal, a total capacitance of the first wire.

13. The machine readable medium of claim 10 wherein a first predetermined signal on the first wire comprises:

evaluating a first periodic current voltage to the first wire via a transistor; and

evaluating a second periodic current voltage to the first wire via an inverter.

14. The machine readable medium of claim 13 wherein the current signal corresponds to current flowing through the transistor.

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